# Toshihiko TAKAHASHI, Ph.D.

Associate Professors
Program: Electrical and Information Engineering
Area: Information Engineering
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## Professional Expertise

His professional expertise encompasses graph algorithms, combinatorics, and VLSI design automation. In this decade, he has investigated representations of floorplans, motivated VLSI layout design. He published “O-tree” representation in 2001, along with co-authors Pei-Ning Guo, Chung-Kuan Cheng, and Takeshi Yoshimura and “FT-Squeeze” representation in 2007, along with co-author Ryo Fujimaki.

## Research Fields of Interest

VLSI Design Automation, Graph Algorithms, and Combinatorics.


Watergate (Not a political scandal in the United States!): Takahashi devised a transistor controlled by water. In 2005, He built and demonstrated a full-adder circuit for children.

## Education

1991: Doctor of Engineering, Tokyo Institute of Technology, Japan
1988: Master of Engineering, Tokyo Institute of Technology, Japan
1985: Bachelor of Engineering, Tokyo Institute of Technology, Japan

## Professional Societies and Activities

1. Member, The Institute of Electrical and Electronics Engineers, Inc. (IEEE)
2. Member, The Institute of Electronics, Information and Communication Engineers (IEICE)
3. Member, Information Processing Society of Japan (IPSJ)

## Awards

1. 2002 IEEE Circuits and Systems CAD Transactions Best Paper Award: "Floorplan Using a Tree Representation," P.-N.Guo, T.Takahashi, C.-K.Cheng, and T.Yoshimura, IEEE Trans. Computer-Aided Design, Vol.20, No.2, pp.281 – 289, 2001.

## Major Publications

### Papers

[1] Inoue, Y., Takahashi, T., and Fujimaki, R., "Counting Rectangular Drawings or Floorplans in Polynomial Time, IEICE Trans. on Fundamentals of Electronics," Communications and Computer Sciences, Vol.E92-A, No.4, pp.1115 – 1120, 2009.

[2] Takahashi, T. and Fujimaki, R., "Fujimaki-Takahashi Squeeze: Linear time construction of constraint graphs of floorplan for a given permutation," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, Vol.E91-A, No.4, pp.1071 – 1076, 2008.

[3] Fujimaki, R. and Takahashi, T., "A Surjective Mapping from Permutations to Room-to- Room Floorplans," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, Vol.E90-A, No.4, pp.823-828, 2007.

[4] Guo., P. -N., Takahashi, T., Cheng, C. -K., and Yoshimura, T., "Floorplan Using a Tree Representation," IEEE Trans. Computer-Aided Design, Vol.20, No.2, pp.281-289, 2001.

[5] Takahashi, T., "Balanced k-Coloring of Polyominos," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, Vol.E77-A, pp. 517-520, 1994.

### Conference Proceedings

[1] Fujimaki, R. and Takahashi, T.. "An Asymptotic Estimate of the Numbers of Rectangular Drawings or Floorplans," Proc. 2009 IEEE International Symposium on Circuits and Systems (ISCAS2009), pp. 856-859, 2009.

[2] Fujimaki, R. and Takahashi, T., "Fujimaki-Takahashi Squeeze: Linear time construction of constraint graphs of floorplan for a given permutation," Proc. The 14th Workshop on Synthesis and System Integration of Mixed Information technologies (SASIMI2007), pp. 208-213, 2007.

[3] Takahashi, T. and Hirabayashi, K., "A New Algorithm for Optimal File Transfer on Path Networks," Proc. 2001 International Technical Conference on Circuits/Systems, Computers and Communication (ITC-CSCC2001), Vol. 1, pp. 324-326, 2001.

[4] Takahashi, T., "Dropping Method for Rectangle Packing Problem," Proc. 2000 IEEE International Symposium on Circuits and Systems(ISCAS2000), pp. 200-203, 2000.

[5] Takahashi, T., "A New Encoding Scheme for Rectangle Packing Problem," Proc. Asia and South Pacific design Automation Conference 2000 (ASP-DAC2000), pp. 175-178, 2000.

[6] Takahashi, T., "A Simple Encoding Scheme for Rectangle Packing Problem," Proc. 1999 International Technical Conference on Circuits/Systems, Computers and Communication
(ITC-CSCC1999), Vol. 1, pp. 352-354, 1999.

[7] Sarrafzadeh, M. and Takahashi, T., "A Fast Algorithm for Routability Testing," Proc. 1999 IEEE International Symposium on Circuits and Systems(ISCAS1999), Vol. 6, pp. 178-181, 1999.

### Book Chapters

[1] Takahashi, T., Fujimaki, R., and Inoue, Y., "A (4n–4)-Bit Representation of a Rectangular Drawing or Floorplan," Lecture Notes in Computer Science, Ngo, H.Q. (Ed.): COCOON 2009, LNCS 5609, pp.47-55, 2009.

[2] Takahashi, T. and Kajitani, Y. 1994, "The Virtual Dimensions of a Straight Line Embedding of a Plane Graph," Algorithmic Aspects of VLSI Layout (Lecture Notes Series on Computing, Vol 2), Sarrafzadeh, M and Lee, D. T. (Ed.), World Scientific Publishing, pp.357-364, 1994.